A7 cont

less than one – two pixels wide including guard rings 103, 208 and space 210. The array of image sensors 99 therefore forms a system where each pixel is separated from each adjacent pixel in the adjacent image sensor by an amount that is small enough to allow interpolation of the missing space, to thereby obtain an uninterrupted image.

Please replace the paragraph beginning on page 5, line 15, and ending on page 5, line 23 with the following new paragraph:

A3

SRAM 304 stores temporary results, and also buffers the information as needed. Connections 306 can couple commands to the row circuitry. The overall chip driver 310 can be the same as conventional, including A/D converters for each column and the like. Element 312 also preferably includes a two-pixel interpolator that is used to interpolate for the missing pixels at areas 105 and 107 and includes pixel interpolation at space 210 caused by rough edges of the butted image sensors. Pixel interpolation is well known in the art, and is described, for example, in US Patent no. 4,816,923. More preferably, the pixel interpolation is done in software.

In the Claims

Please amend claim 1 as follows:

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1. (Amended) A CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of rows and columns, and image sensor logic on said substrate, said logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor other than said rows individually,

said substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge;

said image sensor extending between said first edge, said second edge, and said third edge, such that a first area adjacent said first edge of the chip includes first pixels of the image sensor, a second area adjacent said second edge of the chip includes image sensors, and a third area adjacent said third edge of the chip includes image sensors;

said row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor;

a pixel interpolator and said chip driver circuitry located between said image area and said fourth edge; and

a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate.

Please add claims 9-12 as follows:

9. A CMOS imager, comprising:

a first CMOS image sensor having an image sensor portion arranged in an array of rows and columns, said first CMOS image sensor formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge;

said first CMOS image sensor having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor thereby forming at least two image sensor areas; and

said control portion including a pixel interpolator located between said at least two image sensor area and one of said edges of said image sensor.

10. The CMOS imager according to claim 9, further comprising a second CMOS image sensor configured similarly to said first CMOS image sensor and abutted to one of said edges of said first CMOS image sensor.

11. A method of fabricating a CMOS imager comprising:

fabricating at least two CMOS image sensors having an image sensor portion arranged in an array of rows and columns, said at least two CMOS image sensors formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge, said at least two image sensor having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor thereby forming at least two image sensor areas, said control portion including a pixel interpolator located between said at least two image sensor area and one of said edges of said image sensor;

abutting said at least two CMOS image sensors together; and

integrating said control portions of said at least two CMOS image sensors such that said at least two CMOS image sensors function as a single CMOS imager.

12. The method of fabricating according to claim 11, further comprising interpolating, using said pixel interpolator of said control portion, missing pixels caused by said centralized row-local control portion and by spaces between said at least two image sensors.